IN THE CLAIMS

1. (original) An integrated circuit chip comprising:

a plurality of random access memory (RAM) blocks, wherein each of the RAM blocks is accessible by system circuitry located on the chip during normal operation of the chip;

a plurality of test modules, each being coupled to a corresponding one of the RAM blocks, wherein each of the test modules enables access to a corresponding one of the RAM blocks, independent of the system circuitry; and

a dedicated test bus coupled to each of the test modules.

2. (previously amended) The integrated circuit chip of Claim 1, further comprising:

a plurality of pads; and

a switching structure coupled to the plurality of pads, wherein the switching structure is configured to alternately couple the plurality of pads to the dedicated test bus and the system circuitry.

3. (original) The integrated circuit chip of Claim 2, further comprising a JTAG controller configured to control the switching structure.

4. (original) The integrated circuit chip of Claim 2, wherein the plurality of RAM blocks comprise dual-port and two-port RAM blocks.

5. (original) The integrated circuit chip of Claim 1, wherein the dedicated test bus comprises:

a first set of lines for transmitting address and data signals to the test modules;

a second set of lines for transmitting command signals to the test modules; and

a third set of one or more lines for transmitting a signal for latching the command signals.

6. (original) The integrated circuit chip of Claim 5, wherein the dedicated test bus further comprises a fourth set of lines for transmitting byte-enable signals to the test modules.

7. (original) The integrated circuit chip of Claim 5, wherein the dedicated test bus further comprises a fourth set of lines for transmitting data values from the test modules.

8. (original) The integrated circuit chip of Claim 1, wherein each of the test modules comprises a register for storing a unique address.

9. (original) The integrated circuit chip of Claim 1, wherein each of the RAM blocks includes a multiplexer structure for alternately routing input signals from a corresponding test module or the system circuitry, the multiplexer structure being controlled by a signal from the corresponding test module.

10. (original) The integrated circuit chip of Claim 1, wherein each of the RAM blocks has a capacity of 32 Kb or less.

11. (original) A method of operating RAM blocks having a capacity less of 32 Kb or less embedded in system circuitry on an integrated circuit chip, the method comprising the steps of:

accessing the RAM blocks through the system circuitry during normal operation of the chip; and

accessing the RAM blocks through a dedicated test bus during a test mode to test the functionality of the RAM blocks prior to normal operation of the chip.

12. (original) The method of Claim 11, further comprising the steps of accessing the RAM blocks through dedicated test modules coupled to the test bus during the test mode.

13. (original) The method of Claim 12, further comprising the step of storing a unique address in each of the test modules.

14. (original) The method of Claim 11, wherein the chip comprises a plurality of pads, the method further comprising the steps of:

coupling the pads to the system circuitry during normal operation of the chip; and

coupling the pads to the test bus during the test mode.

15. (original) The method of Claim 14, further comprising the step of controlling the coupling of the pads using a JTAG controller.

16. (original) The method of Claim 11, further comprising the steps of:

writing test data values to the RAM blocks by broadcasting the test data values to all of the RAM blocks on the test bus; and then

reading test data values from the RAM blocks by individually accessing the RAM blocks on the test bus.

17. (original) The method of Claim 16, further comprising the steps of:

writing test data values to RAM blocks having one write port and to the first write port of RAM blocks having more than one write port; and then

writing test data values to the second write port of RAM blocks having more than one write port.

18. (original) The method of Claim 16, further comprising the steps of:

operating the test bus in response to a first clock signal during the test mode; and

operating the RAM blocks in response to a second clock signal during the test mode, wherein the first clock signal and the second clock signal are independent signals.

19. (previously presented) The method of Claim 18, further comprising adjusting edges of the first clock signal relative to edges of the second clock signal.

20. (previously presented) The integrated circuit chip of Claim 1, wherein each of the test modules includes circuitry configured to route addresses received on the dedicated test bus to a corresponding one of the RAM blocks, whereby the corresponding one of the RAM blocks is accessed in response to the routed addresses.

21. (previously presented) The integrated circuit chip of Claim 20, wherein the dedicated test bus comprises a clock line for routing a clock signal to each of the test modules.

22. (previously presented) The integrated circuit chip of Claim 20, wherein each of the test modules further comprises a comparator coupled to receive a unique identification address and the addresses received on the dedicated test bus, wherein the comparator enables a read operation from the corresponding one of the RAM blocks if the unique identification address matches an address received on the dedicated test bus.